REMARKS

Present Status of the Application

The Office Action objected to claim 8, as being an improper dependent claim. Further, the Office Action rejected claims 4 and 26, as being indefinite for the recitation of the phrase "high molecular weight material layer". The Office Action rejected all presently-pending claims 1-8, 17, 18 and 25-30. Specifically, the Office Action rejected claims 1 and 17 under 35 U.S.C. 102(b), as being anticipated by Hong (U.S. 6,037,227), and rejected claims 2-8, 18 and 25-30 under 35 U.S.C. 103(a), as being anticipated by Hong in view of Chan et al. (U.S. 6,440,875). Applicants have amended claims 1, 4, 8, 17, 26 and added claims 31-33 to improve clarity. After entry of the foregoing amendments, claims 1-8, 17, 18 and 25-33 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Summary of Applicant's Invention

The Applicant's invention is directed to a memory device with buried bit lines. The device comprises a substrate, a gate, a gate oxide layer, a deep doped region and a shallow doped region. The gate is disposed on a part of the substrate while the gate oxide layer is disposed between the substrate and the gate. The shallow doped region is disposed in the substrate beside both sides of the gate while the deep doped region is disposed in the substrate under a part of the shallow doped region. The shallow doped region and the deep doped region together serve as a

buried bit line of a memory device, and the dopant concentrations in both the deep doped region and the shallow doped region are about the same.

Discussion of objections

According to the Office Action, claim 8 is objected to, as being an improper dependent claim since it is recite as a method claim and it cannot depend on claim 5 which is a device claim. Applicants have amended claim 8 to a device claim. Withdrawal of the objection is courteously requested.

Claims 4 and 26 are rejected, as being indefinite for the recitation of the phrase "high molecular weight material layer". Applicants respectfully claim that the phrase "high molecular weight material layer" means "polymer layer" claimed in page 6, least line 3-1 and page 7, line 1-3 of the provisional. Applicant has amended the phrase "high molecular weight material layer" to "polymer layer" in claims 4 and 26. Withdrawal of the objection is courteously requested.

Discussion of Office Action Rejections

The Office Action rejected claims 1 and 17 under 35 U.S.C. 102(b), as being anticipated by Hong (U.S. 6,037,227). Claims 2-8, 18 and 25-30 are rejected under 35 U.S.C. 103(a), as being anticipated by Hong in view of Chan et al.

Applicants have amended the independent claims 1 and 17 to more clearly define the method according to the present invention. As amended, claims 1 and 17 respectively recite:

Claim 1 (Currently amended) A buried bit line formed in a substrate of a semiconductor device, comprising

a shallow doped region, disposed in the substrate; and

a deep doped region, disposed in the substrate under a part of the shallow doped region, a deep doped region, disposed in the substrate under a part of the shallow doped region, wherein ***dopant concentrations in the deep doped region and the shallow doped region are about the same,*** and the shallow doped region and the deep doped region together serve as a buried bit line of the memory device.

Claim 17 (Currently amended) A memory device, comprising:

a substrate;

a gate, disposed on a part of the substrate;

a gate oxide layer, disposed between the substrate and the gate;

a shallow doped region, disposed in the substrate beside both sides of the gate; and

a deep doped region, disposed in the substrate under a part of the shallow doped region, wherein ***dopant concentrations in the deep doped region and the shallow doped region are about the same,*** and the shallow doped region and the deep doped region together serve as a buried bit line of the memory device.

Applicants submit that claims 1 and 17 patently define over the prior reference for at least the reason that the cited art fails to disclose at least the features emphasized above.

The buried bit line of the present invention is formed with a shallow doped region and a deep region and *dopant concentrations of the shallow doped region and the deep region are about* ***the same,*** *so that* ***the resistance of the buried bit line of the memory device is effectively lowered.***

Hong, on the other hand, discloses a buried bit line is consist of a first portion 56 with a first dosage of approximately 1×10^{14} /cm^2 and a second portion 60 with a second dosage of approximately 1×10^{15} /cm^2 recited in column 5, line 5-63. In other words, *the dpoant concentration of the second portion 60 is* ***higher than*** *that of the first portion 56*, rather than the dpoant concentration of the second portion 60 is the same as that of the first portion 56. Hence, in Hong, the resistance of the buried bit line of the memory device cannot be effectively lowered. Therefore, Hong fails to teach or suggest all the features of the present invention.

As a result, Applicants submit that amended claims 1 and 17 patently define over the cited references, and should be allowed. For at least the foregoing reasons, all pending claims 2-8, 18, 25-30 patently define over the cited references and should be allowed. Accordingly, the rejection under § 102 and 103 should be withdrawn.

New claims 30-33 are added to further define the invention. The claims are believed allowable and such allowance is respectfully requested

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-8, 17, 18 and 25-33 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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